AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claim 1 as follows:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor integrated circuit comprising a temperature detection circuit including:

a signal output circuit outputting a first signal having at least one rising or falling portion;

a delay circuit <u>connected to the signal output circuit and</u> formed of at least one inverter to output a delayed version of said first signal;

a logic circuit receiving said first signal and said delayed version of said first signal;

a pulse width measurement circuit outputting a signal asserted in response to a signal <u>directly</u> received from said logic circuit having a pulse with a width of no less than a predetermined width corresponding to a temperature desired to be detected; and

a latch circuit latching a signal output from said pulse width measurement circuit, said pulse width measurement circuit having an integration circuit receiving a signal output from said logic circuit and a Schmitt trigger circuit receiving a signal output from said integration circuit, said Schmitt trigger circuit having a trigger potential set to have a value corresponding to said predetermined width.

- 2. (Original) The semiconductor integrated circuit according to claim 1, wherein said delay circuit is arranged external to said semiconductor integrated circuit.
- 3. (Original) The semiconductor integrated circuit according to claim 1, wherein said pulse width measurement circuit is arranged external to said semiconductor integrated circuit.
- 4. (Withdrawn) A semiconductor integrated circuit comprising a temperature detection circuit including:

a signal output circuit outputting a first signal having at least one rising or falling portion;

a plurality of delay circuits connected in series, each formed of at least one inverter to output a delayed version of said first signal;

a plurality of logic circuits each receiving said delayed version of said first signal output from a corresponding one of said delay circuits, and said first signal;

a plurality of pulse width measurement circuits each outputting a signal asserted in response to a signal received from a corresponding one of said logic circuits having a pulse with a width of no less than a predetermined width corresponding to a temperature desired to be detected;

a plurality of latch circuits each latching a signal output from a corresponding one of said pulse width measurement circuits; and

a temperature determination circuit counting a logic value of a signal latched by said plurality of latch circuits, and outputting data corresponding to a value thus counted, as data indicative of temperature.

- 5. (Withdrawn) The semiconductor integrated circuit as recited in claim 4, further comprising a universal asynchronous receiver transmitter circuit converting said data indicative of temperature to serial data for output.
- 6. (Withdrawn) The semiconductor integrated circuit as recited in claim 4, further comprising a control circuit operative in response to said data indicative of temperature having no less than a predetermined value to initialize a state of an internal circuit.
- 7. (Withdrawn) The semiconductor integrated circuit as recited in claim 4, further comprising a control circuit operative in response to said data indicative of temperature having no less than a predetermined value to cause an internal circuit to execute an interrupt process.
- 8. (Withdrawn) The semiconductor integrated circuit as recited in claim 4, comprising a control circuit operative in response to said data indicative of temperature having no less than a predetermined value to allow an internal clock to have a low frequency.

- 9. (Withdrawn) The semiconductor integrated circuit as recited in claim 4, comprising a control circuit operative in response to said data indicative of temperature having no less than a predetermined value to set an internal power supply potential to a low potential.
- 10. (Withdrawn) A semiconductor integrated circuit comprising a temperature detection circuit including:
- a signal output circuit outputting a first signal having at least one rising or falling portion
- a plurality of delay circuits connected in series, each formed of at least one inverter to output a delayed version of said first signal;
- a plurality of switches each receiving said delayed version of said first signal output from a corresponding one of said delay circuits;
- a logic circuit receiving said first signal and said delayed version of said first signal output from a conducting one of said plurality of switches;
- a pulse width measurement circuit outputting a signal asserted in response to a signal received from said logic circuit having a pulse with a predetermined width corresponding to a temperature desired to be detected;
- a latch circuit latching a signal output from said pulse width measurement circuit; and
- a temperature determination circuit successively allowing said plurality of switches to conduct, one at a time, starting from said switch corresponding to said delay circuit located at an preceding stage, said temperature determination circuit

outputting as data indicative of temperature, data corresponding to a number of said switch allowing said asserted, latched signal to be first detected.

- 11. (Withdrawn) The semiconductor integrated circuit as recited in claim 10, further comprising a universal asynchronous receiver transmitter circuit converting said data indicative of temperature to serial data for output.
- 12. (Withdrawn) The semiconductor integrated circuit as recited in claim 10, further comprising a control circuit operative in response to said data indicative of temperature having no less than a predetermined value to initialize a state of an internal circuit.
- 13. (Withdrawn) The semiconductor integrated circuit as recited in claim 10, further comprising a control circuit operative in response to said data indicative of temperature having no less than a predetermined value to cause an internal circuit to execute an interrupt process.
- 14. (Withdrawn) The semiconductor integrated circuit as recited in claim 10, comprising a control circuit operative in response to said data indicative of temperature having no less than a predetermined value to allow an internal clock to have a low frequency.
- 15. (Withdrawn) The semiconductor integrated circuit as recited in claim 10, comprising a control circuit operative in response to said data indicative of

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temperature having no less than a predetermined value to set an internal power supply potential to a low potential.